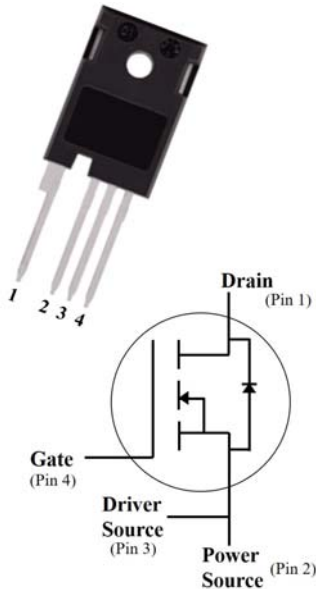


## Silicon Carbide Power MOSFET (N-Channel Enhancement)

$V_{DS}$	1200V
$I_D$ (25°C)	80A
$R_{DS(on)}$	25mΩ



### Features

- High speed switching
- Essentially no switching losses
- Reduction of heat sink requirements
- Maximum working temperature at 175 °C
- High blocking voltage
- Fast Intrinsic diode with low recovery current
- High-frequency operation
- Halogen free, RoHS compliant
- AEC-Q101 qualified

### Typical Applications

Typical applications are in power factor correction(PFC), solar inverter, uninterruptible power supply, motor drives, photovoltaic inverter, electric car and charger.

### Mechanical Data

- **Package:** TO-247-4L
- **Terminals:** Tin plated leads
- **Polarity:** As marked

### ■ Maximum Ratings ( $T_c=25^\circ\text{C}$ Unless otherwise specified)

PARAMETER	SYMBOL	UNIT	VALUE	TEST CONDITIONS	NOTE
Device marking code			D212025NCFYG3Q		
Drain source voltage @ $T_j=25^\circ\text{C}$	$V_{DS,max}$	V	1200	$V_{GS}=0\text{V}$ , $I_D=100\mu\text{A}$	
Gate source voltage @ $T_j=25^\circ\text{C}$	$V_{GS,max}$	V	-8/+22	Absolute maximum values	
Gate source voltage @ $T_j=25^\circ\text{C}$	$V_{GS,op}$	V	-4/+18	Recommended operational values	
Continuous drain current @ $T_c=25^\circ\text{C}$	$I_D$	A	80	$V_{GS}=18\text{V}$ , $T_c=25^\circ\text{C}$	Fig.17
Continuous drain current @ $T_c=100^\circ\text{C}$			55	$V_{GS}=18\text{V}$ , $T_c=100^\circ\text{C}$	
Pulsed drain current	$I_{D(pulsed)}$	A	178	Pulse width $t_p$ limited by $T_{j,max}$	Fig.22
Avalanche energy, Single pulse	$E_{AS}$	J	1.1	$V_{DD}=75\text{V}$ , $L=30\text{mH}$	
Power Dissipation	$P_{TOT}$	W	365	$T_c=25^\circ\text{C}$ , $T_j = 175^\circ\text{C}$	Fig.16
Power Dissipation			182	$T_c=100^\circ\text{C}$ , $T_j = 175^\circ\text{C}$	
Operating junction and Storage temperature range	$T_j, T_{stg}$	$^\circ\text{C}$	-55 to +175		
Soldering temperature	$T_L$	$^\circ\text{C}$	260	1.6mm (0.063") from case for 10s	
Mounting torque	$T_M$	Nm	0.6	M3 screw Maximum of mounting process: 3	



## ■Static Electrical Characteristics (Tc=25°C unless otherwise specified)

PARAMETER	SYMBOL	UNIT	Min.	Typ.	Max.	Test Conditions	Note
Gate threshold voltage	$V_{GS(th)}$	V	2.0	2.7	4.0	$V_{DS}=V_{GS}, I_D=15mA$	Fig.4, 11
				2.0		$V_{DS}=V_{GS}, I_D=15mA, T_J=175^\circ C$	
Drain source breakdown voltage	$V_{(BR)DSS}$	V	1200			$V_{GS}=0V, I_D=100\mu A$	
Gate source leakage current	$I_{GSS}$	nA		10	100	$V_{GS}=18V, V_{DS}=0V$	
Current drain source on-state resistance	$R_{DS(on)}$	mΩ		25	40	$V_{GS}=18V, I_D=40A$	Fig.5, 6, 7
				46		$V_{GS}=18V, I_D=40A, T_J=175^\circ C$	
Transconductance	$g_f$	S		28		$V_{DS}=20V, I_D=40A$	Fig.4
				26		$V_{DS}=20V, I_D=40A, T_J=175^\circ C$	

## ■Dynamic Electrical Characteristics (Tc=25°C unless otherwise specified)

PARAMETER	SYMBOL	UNIT	Min.	Typ.	Max.	Test Conditions	Note
Input capacitance	$C_{iss}$	pF		4710		$V_{DS}=800V, V_{GS}=0V, T_J=25^\circ C$ , $f=100kHz, V_{AC}=25mV$	Fig.13, 14
Output capacitance	$C_{oss}$			160			
Reverse capacitance	$C_{rss}$			6.8			
Coss stored energy	$E_{oss}$	uJ		84			Fig.15
Gate source charge	$Q_{gs}$	nC		40		$V_{DS}=800V, V_{GS}=-4/18V, I_D=40A$	Fig.12
Gate drain charge	$Q_{gd}$			61			
Gate charge	$Q_g$			152			
Internal gate resistance	$R_g$	Ω		2		$f=1MHz$	

## ■Switching Characteristics (Tc=25°C unless otherwise specified)

PARAMETER	SYMBOL	UNIT	Min.	Typ.	Max.	Test Conditions	Note
Turn on switching energy	$E_{on}$	uJ		580		$V_{DD}=800V, V_{GS}=-4/+18V, I_D=40A,$ $R_g=2.4\Omega, L=100\mu H$	Fig.19, 20
Turn off switching energy	$E_{off}$			249			
Turn on delay time	$t_{d(on)}$	ns		19		$V_{DD}=800V, V_{GS}=-4/+18V, I_D=40A,$ $R_g=2.4\Omega, L=100\mu H$	Fig.21
Rise time	$t_r$			37.5			
Turn off delay time	$t_{d(off)}$	ns		25			
Fall time	$t_f$			14			

## ■Body diode characteristics (Tc=25°C unless otherwise specified)

PARAMETER	SYMBOL	UNIT	Min.	Typ.	Max.	Test Conditions	Note
Diode forward voltage	V <sub>SD</sub>	V		4.8		V <sub>GS</sub> =-4V, I <sub>SD</sub> =20A	Fig.8
				3		V <sub>GS</sub> =0V, I <sub>SD</sub> =20A, T <sub>J</sub> =175°C	Fig.9
Continuous diode forward current	I <sub>s</sub>	A		70		T <sub>c</sub> =25°C	
Reverse recovery time	t <sub>rr</sub>	nS		48		V <sub>R</sub> =800V, V <sub>GS</sub> =-4V, I <sub>D</sub> =40A, di/dt=2500A/uS	
Reverse recovery charge	Q <sub>rr</sub>	nC		323			
Peak reverse recovery current	I <sub>rrm</sub>	A		11			

## ■Thermal Characteristics (T<sub>a</sub>=25°C Unless otherwise specified)

PARAMETER	SYMBOL	UNIT	Typ.
Thermal resistance	R <sub>θJ-C</sub>	°C/W	0.41

## ■Typical Characteristics

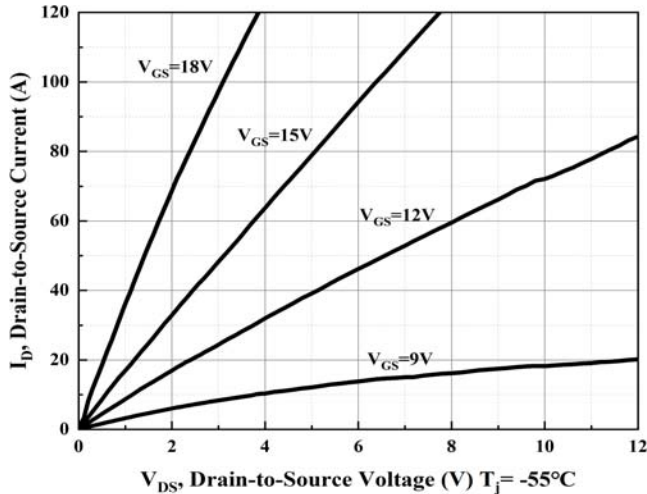


Figure 1. Output Characteristics T<sub>j</sub> = -55°C

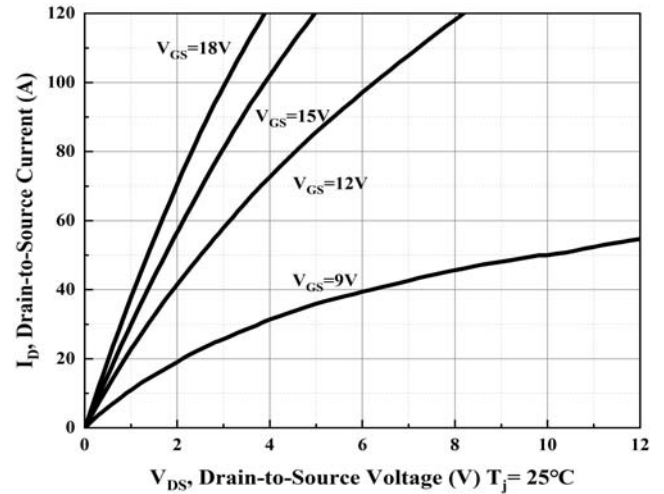


Figure2. Output Characteristics T<sub>j</sub> = 25°C

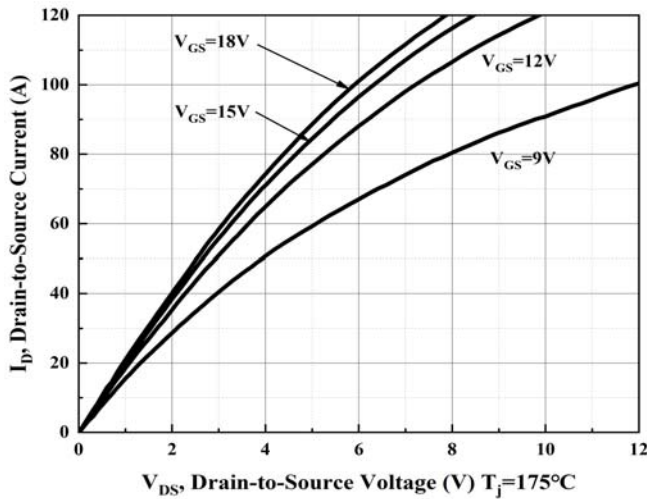


Figure 3. Output Characteristics  $T_j = 175^\circ\text{C}$

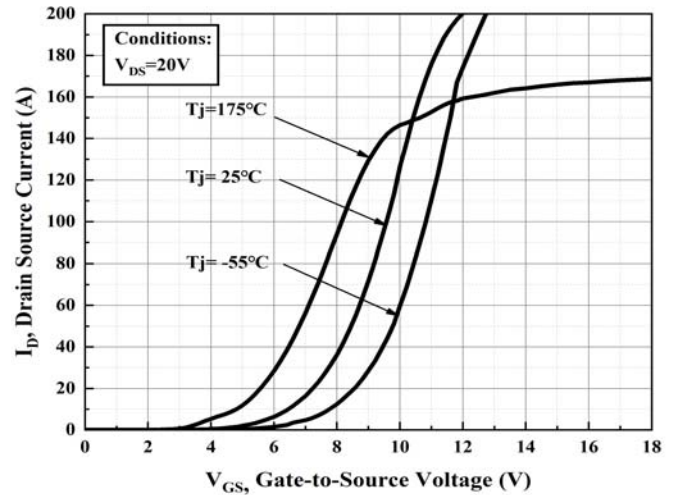


Figure 4. Transfer Characteristics for Various Junction Temperature

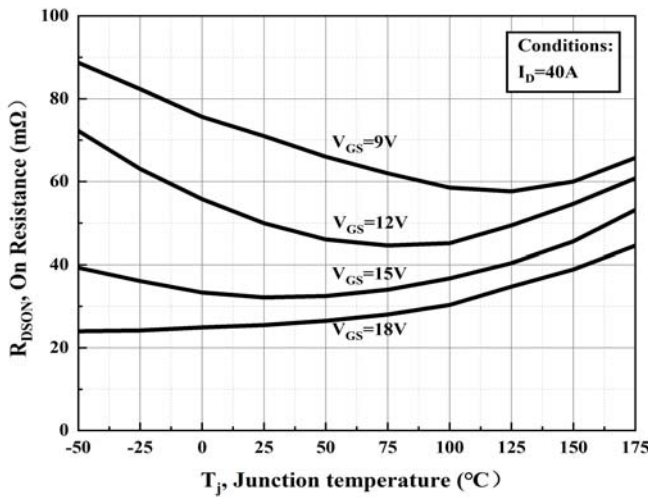


Figure 5. On-resistance vs. Temperature for Various Gate Voltage

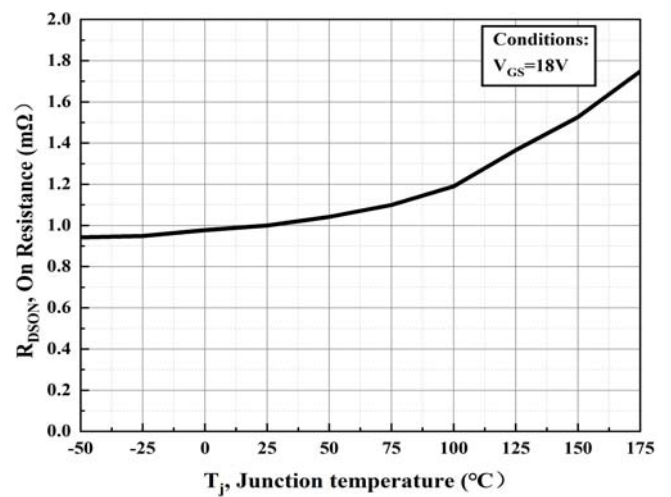


Figure 6. Normalized on-resistance vs. Temperature

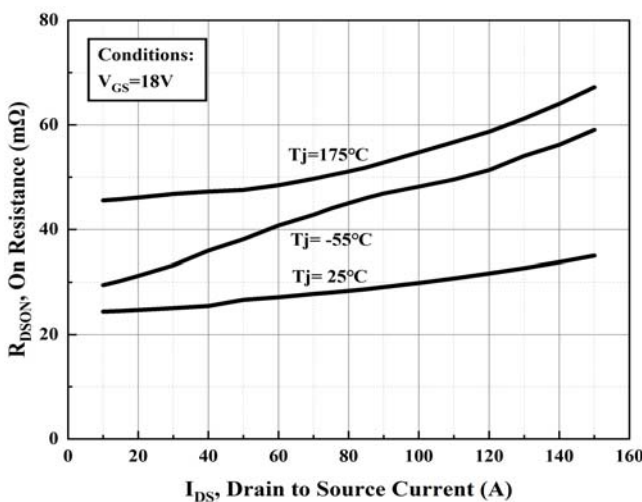


Figure 7. On-resistance vs. Drain Current

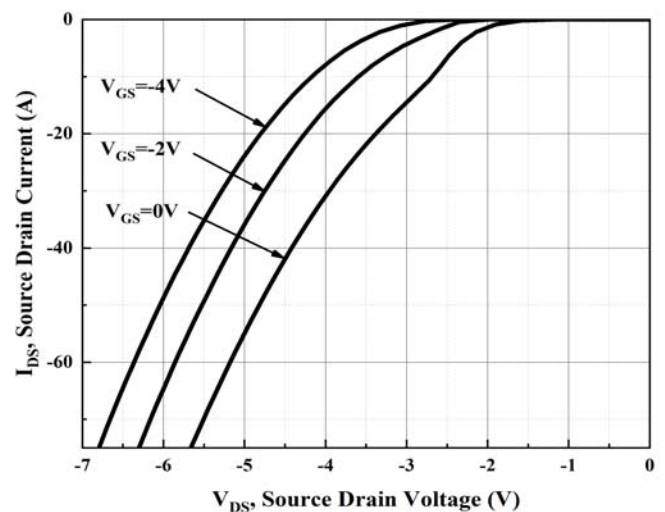


Figure 8. Body Diode Characteristic at  $T_j = 25^\circ\text{C}$

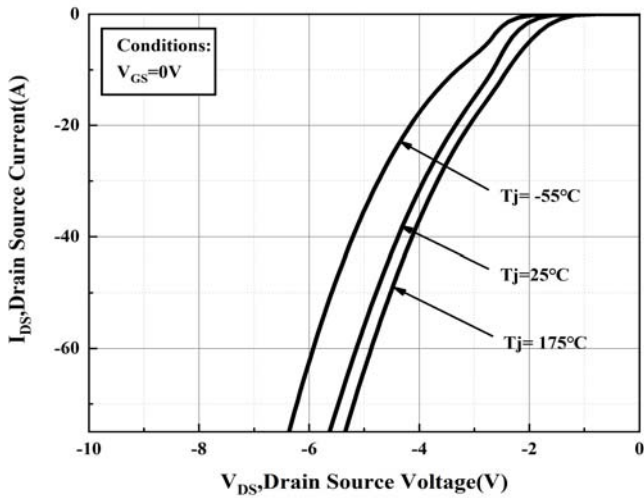


Figure 9. Body Diode Characteristic

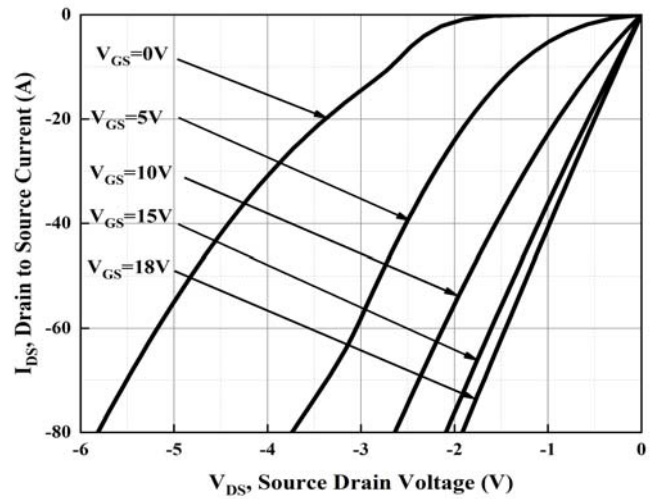


Figure 10. 3<sup>rd</sup> quadrant Characteristic at  $T_j = 25^\circ\text{C}$

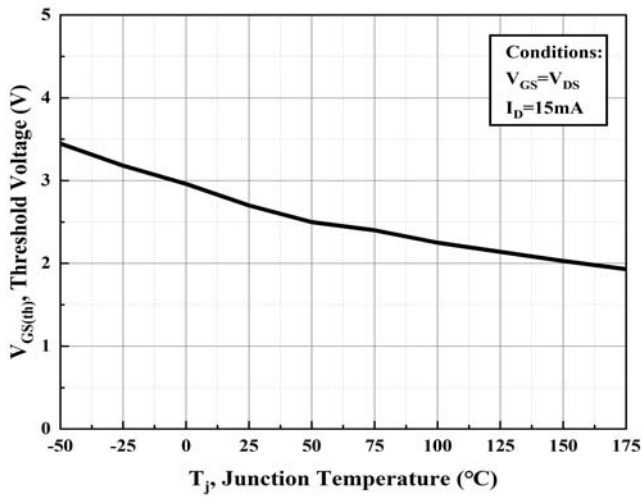


Figure 11. Threshold Voltage vs. Temperature

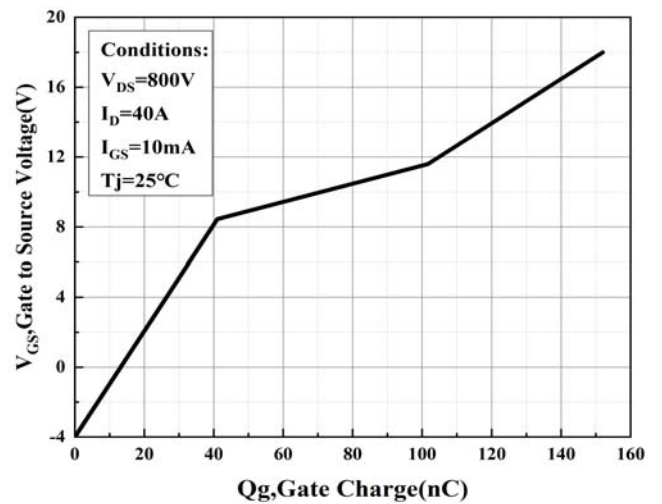


Figure 12. Gate Charge Characteristic

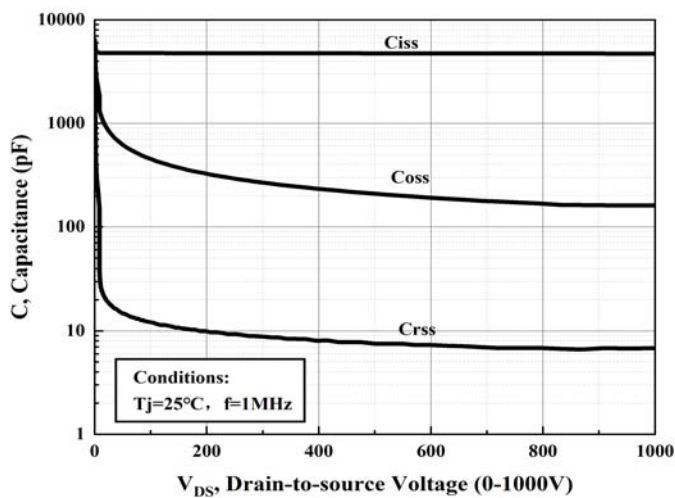


Figure 13. Capacitances vs. Drain Source Voltage (0-1000V)

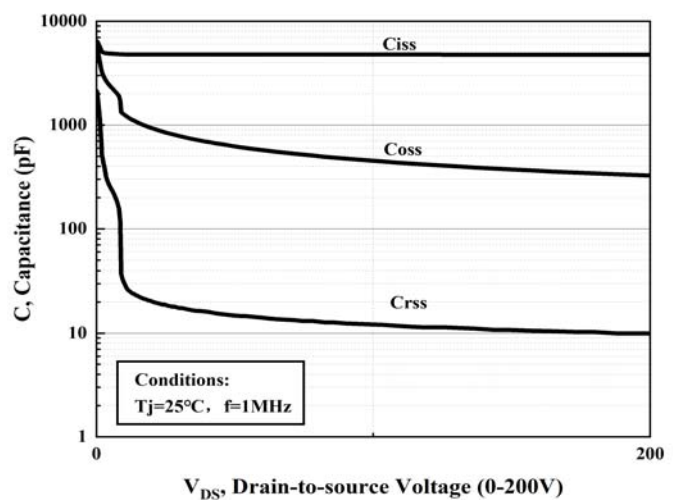


Figure 14. Capacitances vs. Drain Source Voltage (0-200V)

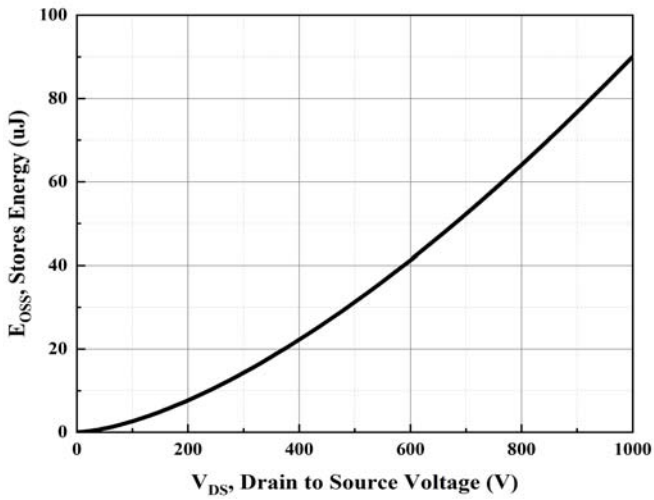


Figure 15. Output Capacitor Stored Energy

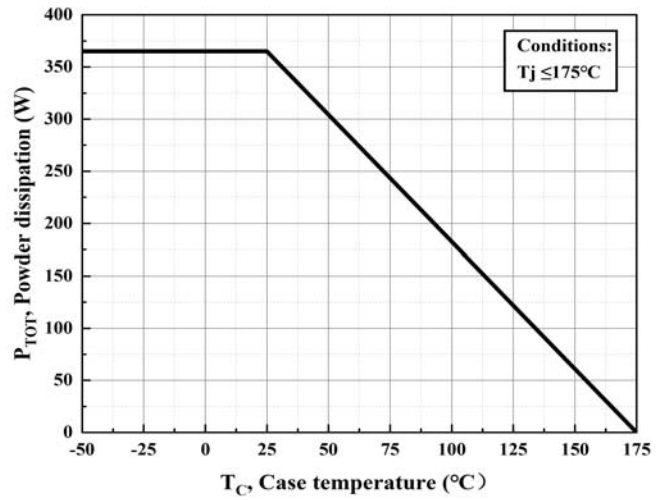


Figure 16. Maximum Power Dissipation Derating vs. Case Temperature

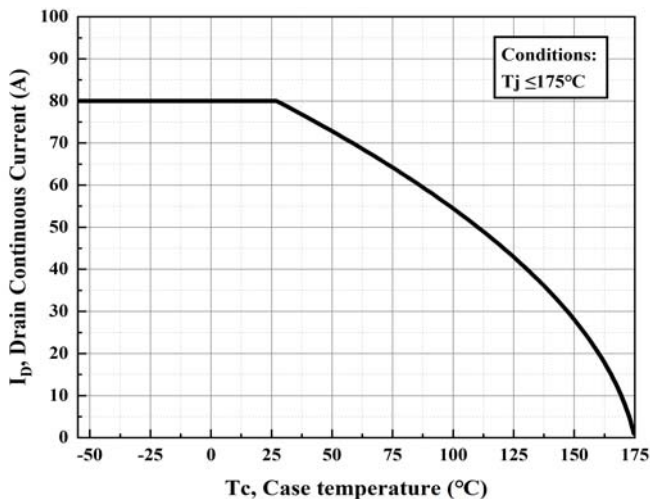


Figure 17. Continuous Drain Current Derating vs. Case Temperature

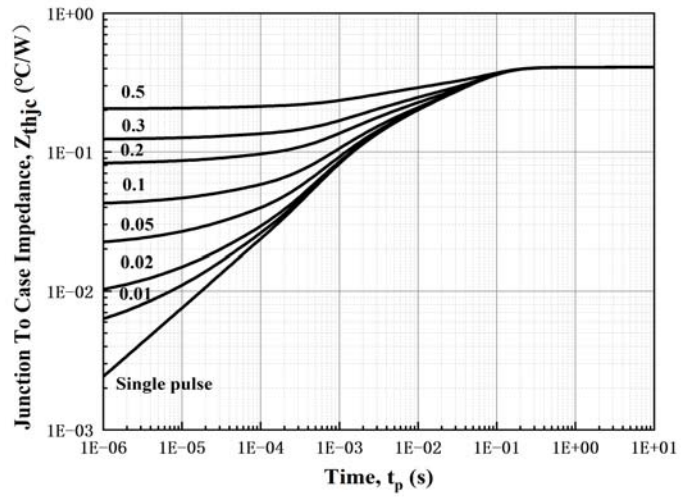


Figure 18. Transient Thermal Impedance (Junction - Case)

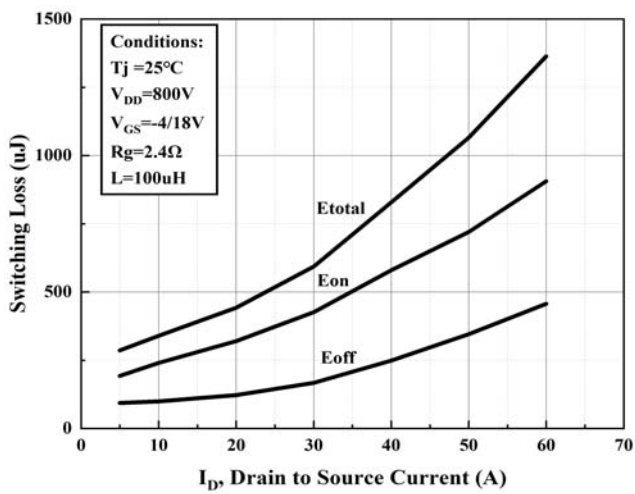


Figure 19. Clamped Inductive Switching Energy vs. Drain Current

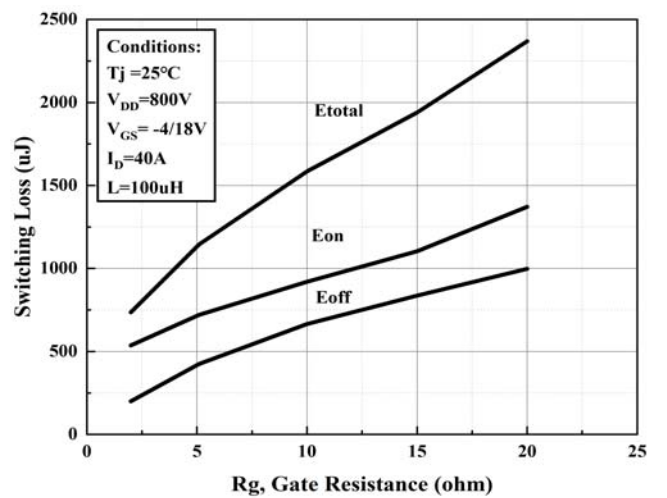


Figure 20. Clamped Inductive Switching Energy vs. Rg

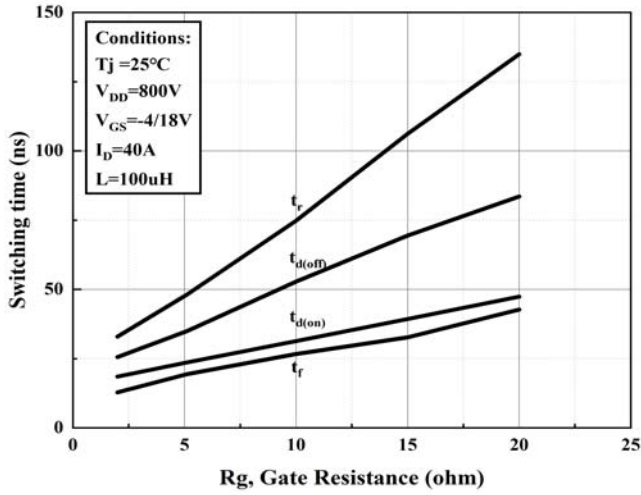


Figure 21. Switching Times vs. Rg

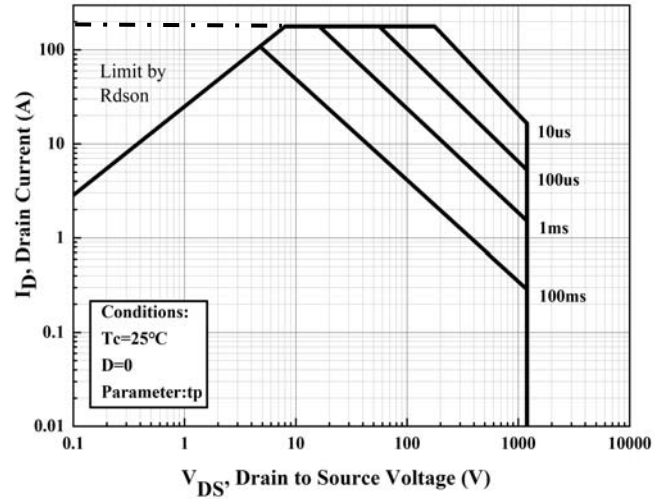


Figure 22. Safe Operating Area

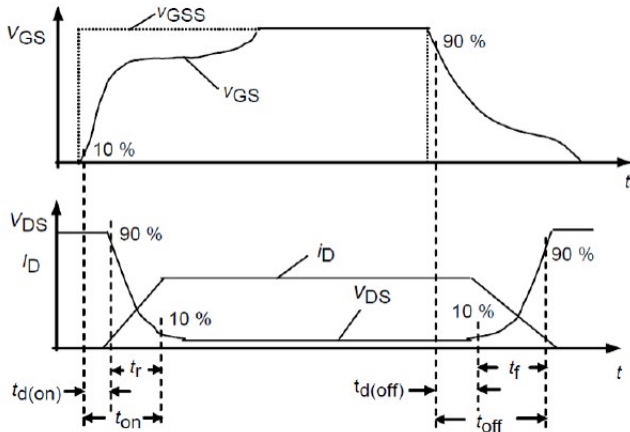


Figure 23. Switching Times Definition

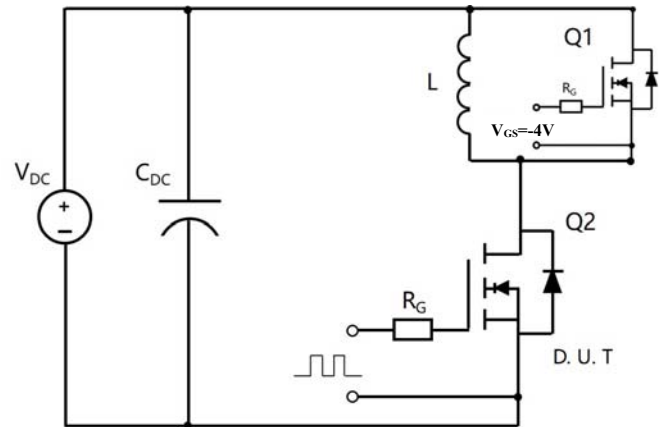
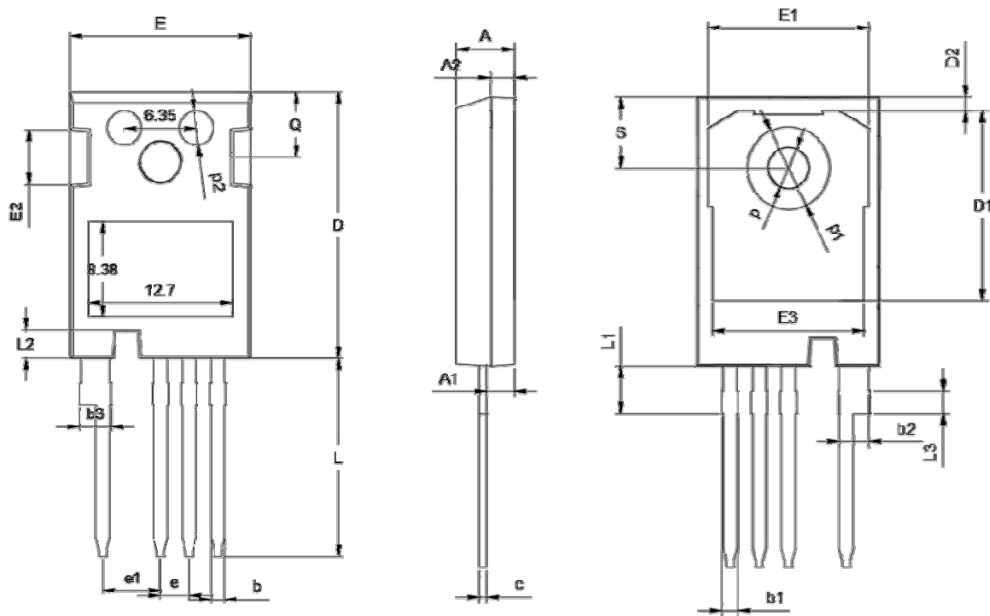


Figure 24. Clamped Inductive Switching Waveform Test Circuit

## ■Outline Dimensions



TO247-4L			
Dim	Min	Norm	Max
A	4.80	5.00	5.20
A1	2.30	2.40	2.50
A2	1.88	1.98	2.08
b	1.10	1.20	1.30
b1	1.20	/	1.50
b2	2.35	2.55	2.75
b3	2.45	/	2.85
c	0.55	0.60	0.65
D	23.3	23.45	23.6
D1	16.25	16.55	16.85
D2	1.00	/	1.30
e	TYP2.54		
e1	TYP5.06		
E	15.75	15.90	16.05
E1	13.80	/	14.20
E2	4.40	4.75	5.10
E3	13.00	/	13.45
L	17.34	17.49	17.64
L1	4.00	/	4.30
L2	2.35	/	2.65
L3	TYP1.98		
Q	5.60	5.80	6.00
S	6.05	/	6.30
p	TYP3.58		
p1	TYP7.18		
p2	TYP3.00		





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